

D 13115

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Name.....

Reg. No.....

FIRST SEMESTER M.Sc. DEGREE (REGULAR/SUPPLEMENTARY)  
EXAMINATION, NOVEMBER 2021

(CBCSS)

Computer Science

CSS 1C 05—COMPUTER ORGANIZATION AND ARCHITECTURE

(2019 Admission onwards)

Time : Three Hours

Maximum : 30 Weightage

General Instructions

1. In cases where choices are provided, students can attend **all** questions in each section.
2. The minimum number of questions to be attended from the Section / Part shall remain the same.
3. The instruction if any, to attend a minimum number of questions from each sub section / sub part / sub division may be ignored.
4. There will be an overall ceiling for each Section / Part that is equivalent to the maximum weightage of the Section / Part.

Section A

Answer any **four** questions.

Each question carries 2 weightage.

1. Draw labelled block diagram and excitation table for J K Flip Flop.
2. Draw full Adder circuit using logic gates.
3. Explain "microinstructions" with an example.
4. Explain the concept of bit pair recoding.
5. Explain 'daisy chaining'.
6. What are the different types of 8086 instructions ? Give one example each.
7. Give an example Timing Diagram based on 8085 instruction set.

$(4 \times 2 = 8 \text{ weightage})$

VM

2x5

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**Section B**

Answer any four questions.  
Each question carries 3 weightage.

1010



8. Simplify using K-map:  $F(P, Q, R, S) = \Sigma(1, 2, 4, 7, 10, 12, 13, 15)$ .
9. With the help of a block diagram, explain the working of Serial-In, Serial-Out shift register.
10. Illustrate how instructions are executed in a single bus architecture.
11. Summarize Booth's Algorithm.
12. Explain the working principle of cache memory. Illustrate any one cache mapping technique.
13. Outline the organization of a DRAM memory cell. Identify different types of DRAM.
14. Write a note on 8051 instruction set.

(4 x 3 = 12 weightage)

EA = A + R

**Section C**

Answer any two questions.  
Each question carries 5 weightage.

Books

15. Discuss the organization of hardwired control unit. Compare it with microprogrammed control unit.
16. With the help of block diagrams explain 'Fast Adders' and 'Sequential Multipliers'.
17. Give a detailed account of programmed I/O, interrupt driven I/O and DMA.
18. Give an overview of 8085 architecture and addressing modes.

MRB  
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